RAYYAN AKBAR

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Digital Design & Verification — Verilog RTL · self-checking testbenches · Python test automation · silicon & system validation

EDUCATION

University of Toronto — BASc, Electrical & Computer Engineering Expected 2028

- Available for 12–16 month PEY Co-op starting May 2027. Relevant coursework: digital systems, computer organization (Nios V / DE1-SoC), circuits, embedded systems, engineering design (APS 112).

TECHNICAL SKILLS

Design & Verification: Verilog-2001 RTL, self-checking testbenches, Python golden-model co-verification, simulation & waveform debug, Quartus Prime, OpenLane RTL-to-GDSII, SkyWater SKY130 PDK, timing closure fundamentals

Validation & Lab: high-speed oscilloscope signal analysis, waveform generators, multimeters, automated bench measurement, PCB bring-up & debug, MPLS telecom link testing

Scripting & Automation: Python (test automation, data processing), shell scripting, Linux, Git

Hardware & Protocols: Altium Designer, I²C, PS/2, VGA, Profibus, Siemens PLCs, MPU-6050 IMU, soldering & board-level rework

EXPERIENCE

Siemens — Engineering Intern, Substation Automation & Telecom [Month Year] – [Month Year]

Saudi Electric Company — Rumah A & B substation projects

- Developed a **Python automation script** that replaced a ~2-day manual SAS gateway configuration process with a **~5-minute automated, repeatable run**, eliminating manual configuration errors.
- Performed **high-speed signal testing and validation** on **MPLS telecom links** using a specialized oscilloscope as part of formal verification & validation of substation communications.
- Wrote Python scripts to automate **device testing and configuration** across the substation automation system (SAS) equipment fleet.
- Owned **hardware selection, verification, assembly, integration testing, and debugging** of SAS and telecom hardware for two grid substations.

Tetra Pak — Engineering Intern, Controls & Automation [Month Year] – [Month Year]

- Replaced a legacy temperature controller on production equipment and added new functionality: **integration with a Siemens PLC over Profibus**; validated PLC behavior post-integration.
- Built a **computer-vision / ML defect recognition system** for printer rolls, automating a previously manual quality inspection step.
- Automated validation and test workflows with **Python and shell scripting in Linux**.

PROJECTS

Tiny Tapeout Digital ASIC — SkyWater SKY130 Fabricated silicon

- Designed Verilog RTL and took it through the full **OpenLane RTL-to-GDSII flow** (synthesis, place & route, CTS, DRC/LVS signoff) on the SKY130 130 nm PDK; design taped out and fabricated.

Binarized Neural Network FPGA Accelerator — MNIST Verilog · DE1-SoC

- Built a BNN inference accelerator in Verilog classifying MNIST digits, including digits drawn live via a **PS/2 mouse** input path with VGA display.
- Verified RTL with **self-checking testbenches against a bit-accurate Python golden model** — automated pass/fail checking mirroring industry reference-model DV methodology.

SDR Quadrature Receiver & Mixer Subsystem PCB Altium · bench-validated

- Designed, hand-soldered, and brought up a quadrature receiver/mixer PCB; measured **38 dB gain** and **90° ±12.5° I/Q phase match**.
- Automated bench characterization with **Python-scripted test sweeps** using oscilloscope, waveform generator, and multimeter; validated the subsystem within the full SDR system.

MPU-6050 Motion-Controlled FPGA Game Verilog · I²C · VGA

- Wrote a custom **I²C master in Verilog** to stream 6-axis accelerometer/gyroscope data from an MPU-6050, conditioning raw sensor data in hardware to drive real-time VGA gameplay.

ADDITIONAL

- Licensed an **LLM-based end-to-end publishing automation platform** (Python) to a media outlet for production use; founded a phone & computer repair service during the pandemic; designed the electrical system for a sound-isolation solution for U of T's OISE Library (APS 112 client design project).